

**SPECIFICATION
FOR
EPD Module**

MODULE No:	KD037WQFSN002
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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1. Over View

KD037WQFSN002 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The 3.7” active area contains 240x416 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- 240×416 pixels display
- White reflectance above 30%
- Contrast ratio above 8:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Landscape, portrait modes
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C signal master interface to read external temperature sensor

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3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	3.7	Inch	
Display Resolution	240(H) x 416(V)	Pixel	
Active Area	47.04(H) x 81.536(V)	mm	
Pixel pitch	0.196(H) x 0.196(V)	mm	
Pixel Configuration	Rectangle		
Outline Dimension	53(H) x 92.99(V) x 1.14(D)	mm	
Module Weight	11	g	
Controller IC	UC8253		
Interface	3Wire / 4Wire SPI	-	
Display mode	EPD,B / W	-	
Operating temperature	0~+50	°C	
Storage temperature	-25~+60	°C	

5. Input/Output Pin Assignment

NO.	Name	DISCRIPTION	I/O	Remark
1	NC	NO Connection	-	Keep open
2	GDR	N-Channel MOSFET Gate Drive Control	O	
3	RESE	Current Sense Input for the Control Loop	I	
4	NC	NO Connection	-	Keep open
5	VDHR	Positive Source driving voltage 1	C	
6	TSCL	IIC Interface to digital temperature sensor Clock pin	O	
7	TSDA	IIC Interface to digital temperature sensor Data pin	I/O	
8	BS	Bus Interface selection pin	I	Note 5-5
9	BUSYN	Busy state output pin	O	Note 5-4
10	RSTN	Reset signal input. Active Low.	I	Note 5-3
11	D/C	Data /Command control pin	I	Note 5-2
12	CSB	Chip select input pin	I	Note 5-1
13	SCL	Serial Clock pin (SPI)	I	
14	SDA	Serial Data pin (SPI)	I/O	
15	VDD	Power Supply for interface logic pins	P	
16	VDD	Power Supply for the chip	P	
17	VSS	Ground	P	
18	VDDD	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	C	
19	VPP	FOR TEST	P	
20	VSH	Positive Source driving voltage 2	C	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH1	C	
22	VSL	Negative Source driving voltage	C	
23	VGL	Power Supply pin for Negative Gate driving voltage VCOM and VSL	C	
24	VCOM	VCOM driving voltage	C	

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I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output),
P = Power Pin, C =Capacitor Pin

Note 5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled Low.

Note 5-2: This pin (D/C) is Data/Command control pin connecting to the MCU in 4 -wire SPI mode. When the pin is pulled High, the data at SDA will be interpreted as data. When the pin is pulled Low, the data at SDA will be interpreted as command.

Note 5-3: This pin (RSTN) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when
- Outputting display waveform
-Communicating with digital temperature sensor.

Note 5-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is “Low” , 4-line SPI is selected. When it is “High” , 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{dd}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to $V_{dd} + 0.5$	V
Logic Output voltage	V_{OUT}	-0.5 to $V_{dd} + 0.5$	V

Note: Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

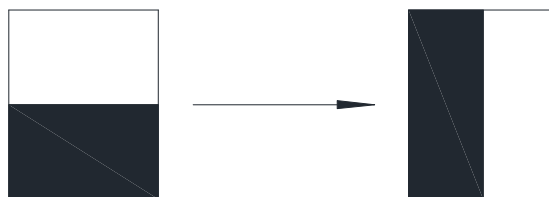
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6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, TOPR =23°C

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V _{SS}	-		-	0	-	V
Logic supply voltage	V _{DD}	-	VDD	2.4	3.0	3.6	V
High level input voltage	V _{IH}	-	-	0.8 V _{DD}	-	-	V
Low level input voltage	V _{IL}	-	-	-	-	0.2V _{DD}	V
High level output voltage	V _{OH}	I _{OH} = -100uA	-	0.9 V _{DD}	-	-	V
Low level output voltage	V _{OL}	I _{OL} = 100uA	-	-	-	0.1V _{DD}	V
OTP Program voltage	V _{pp}	-	VPP	-	8.25	-	V
Typical power panel	P _{TYP}	-	-	-	15	210	mW
Deep sleep mode	P _{STPY}	-	-	-	3	-	mW
Typical operating current	I _{opr_VDD}	V _{DD} =3.0V	-	-	5	70	mA
Sleep mode current	I _{slp_VDD}	DC/DC off No clock No input load Ram data retain	VDD	-	26	-	uA
Deep sleep mode current	I _{dslp_VDD}	DC/DC off No clock No input load Ram data not retain	VDD	-	1	-	uA

Notes:1.The typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.



2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

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6.3 AC Characteristics

6.3.1 MCU Interface selection

The pin assignment at different interface mode is summarized in Table. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
	SDA	SCL	CSB	D/C	RSTN
Bus interface	SDA	SCL	CSB	D/C	RSTN
BS=L 4-wire SPI	SDIN	SCLK	CSB	D/C	RSTN
BS=H 3-wire SPI	SDIN	SCLK	CSB	L	RSTN

6.3.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C and CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

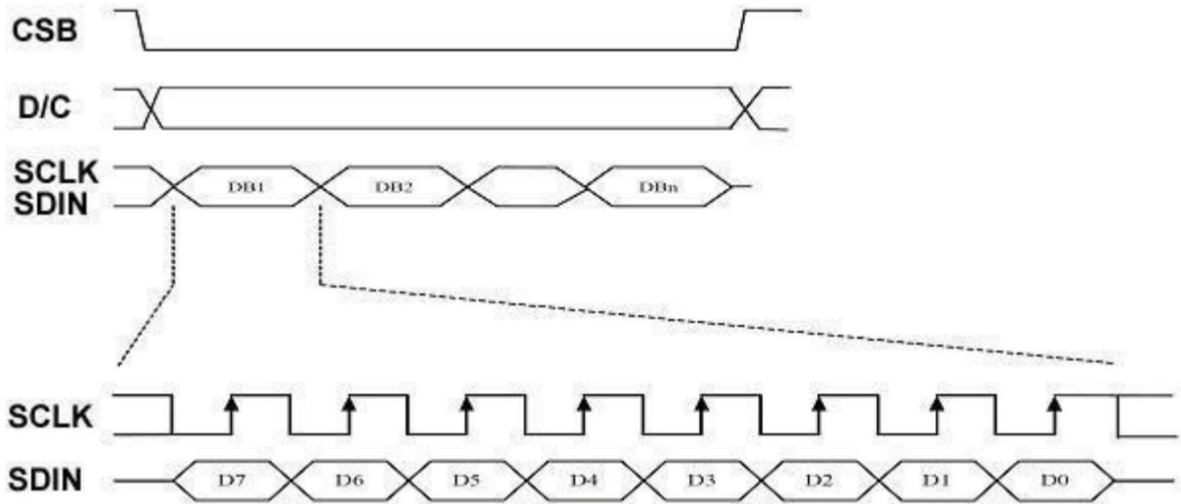
Function	CSB	D/C	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note:

(1) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.



Write procedure in 4-wire SPI mode

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6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCLK, serial data SDIN and CSB.

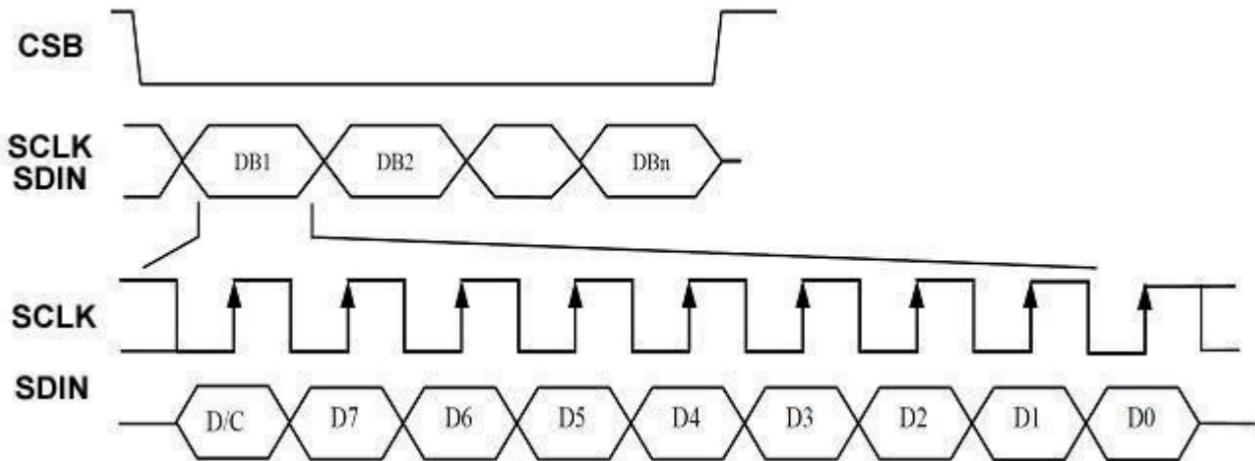
In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

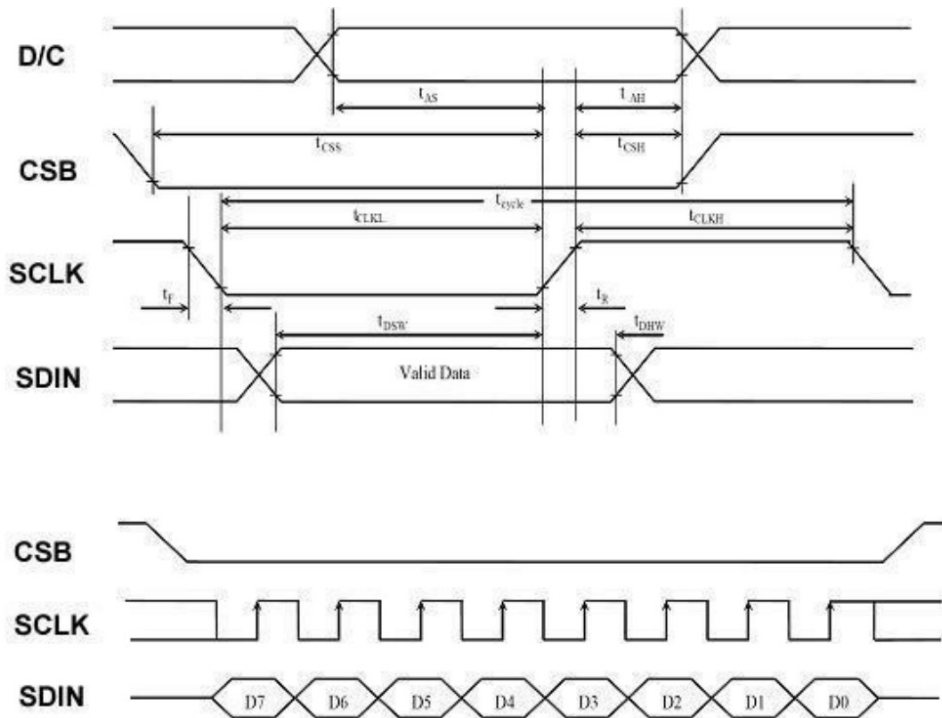
Under serial mode, only write operations are allowed.



Write procedure in 3-wire SPI mode

6.3.4 Interface Timing

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR}=25°C



Serial interface characteristics

(V_{DD} - V_{SS} = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Serial Interface Timing Characteristics

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7. Optical Characteristics

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	7-1
CR	Contrast Ratio		8.1	10.1	-		7-2
White L 24h	Reduce	-		≤4	-		
T _{update}	Image update time	at 25 °C		2800	-	ms	

Notes: 7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

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8. Handling, Safety and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System(IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other Conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

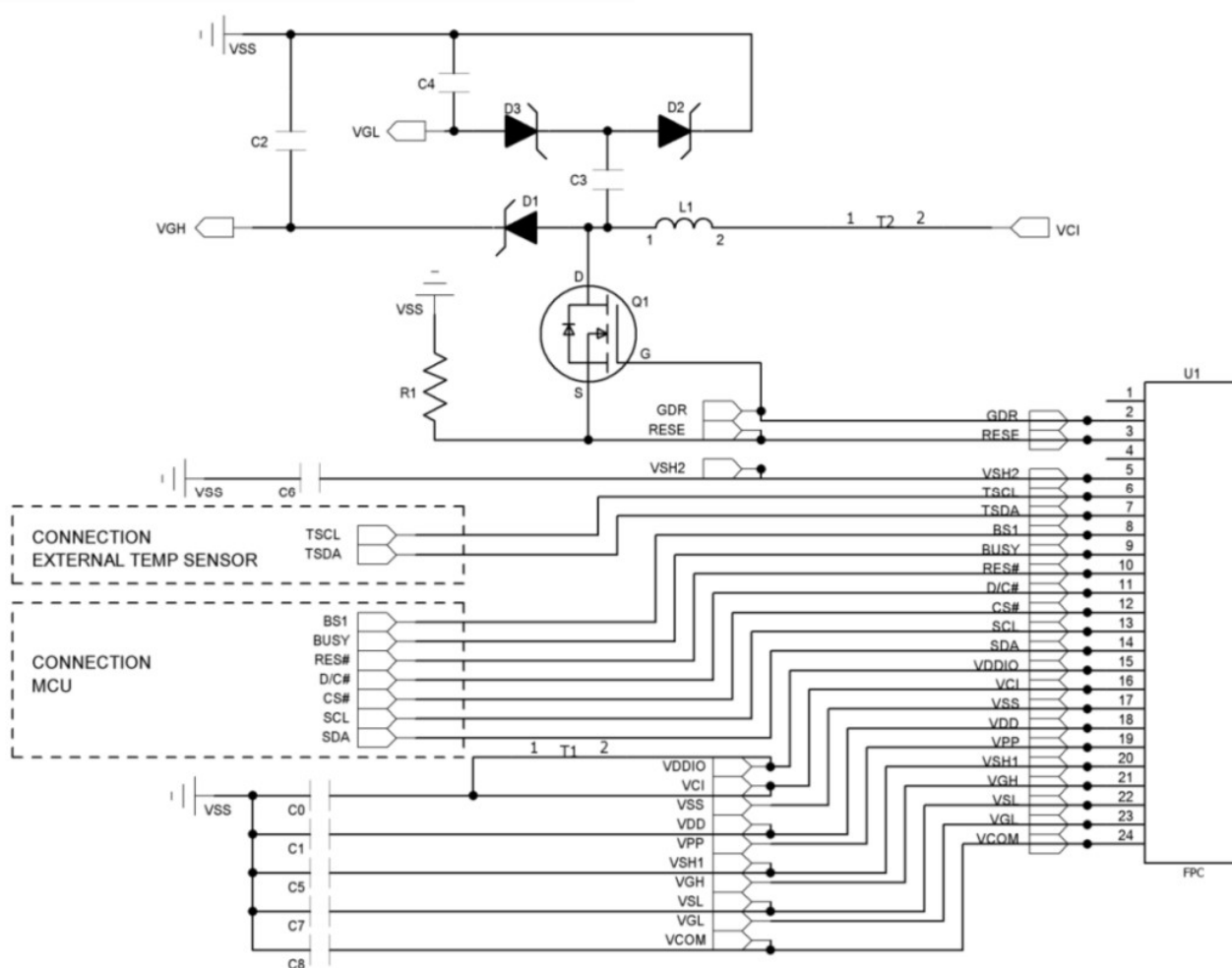
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9. Reliability test

NO.	Test items	Test condition	Method	Remark
1	High-Temperature Operation	T=50°C, RH=30%, 240 h	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T=+70°C, RH=23%, 240 h	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C, 240 h	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature High-Humidity Operation	T=+40°C, RH=90%, 168 h	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature High Humidity Storage	T=+60°C, RH=80%, 240 h	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1cycle:[-25°C 30min]→ [+70°C 30min]: 100cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full Packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence:1 corner, 3edges, 6 faces One drop for each	Full Packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

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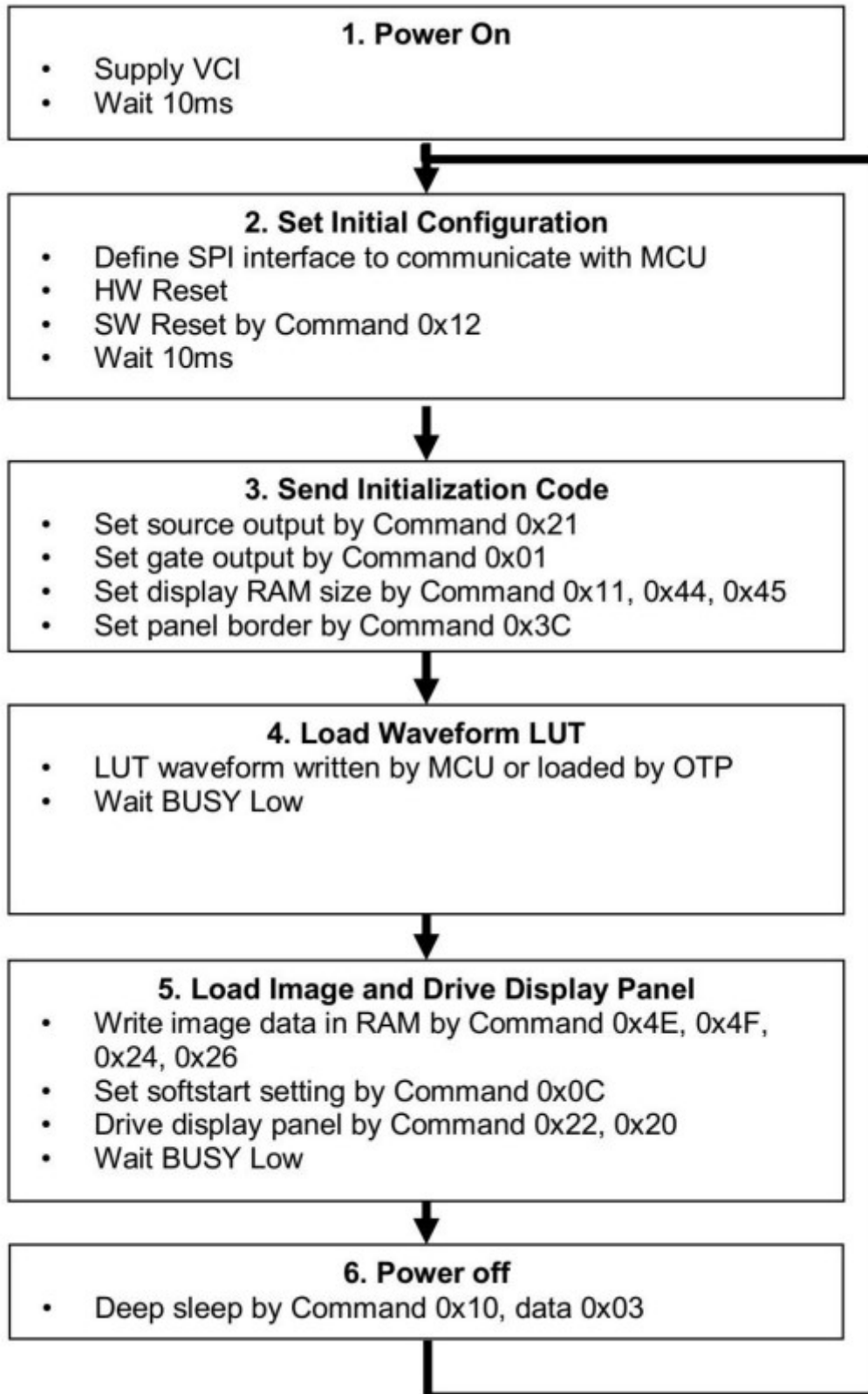
10. Typical Application Circuit with SPI Interface



Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2 ohm	0402/0603/0805; 1% variation, $\geq 0.05W$
D1-D3	Diode	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) $I_o \geq 500mA$ 3) Forward voltage $\leq 430mV$
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs(th)} = 0.9V$ (Typ), 1.3V (Max) 3) $R_{ds\ on} \leq 2.1\Omega$ @ $V_{gs} = 2.5V$
L1	47uH	CDRH2D18 / LDNP-470NC $I_o = 500mA$ (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

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11. Typical Operating Sequence



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12. Inspection condition

12.1 Environment

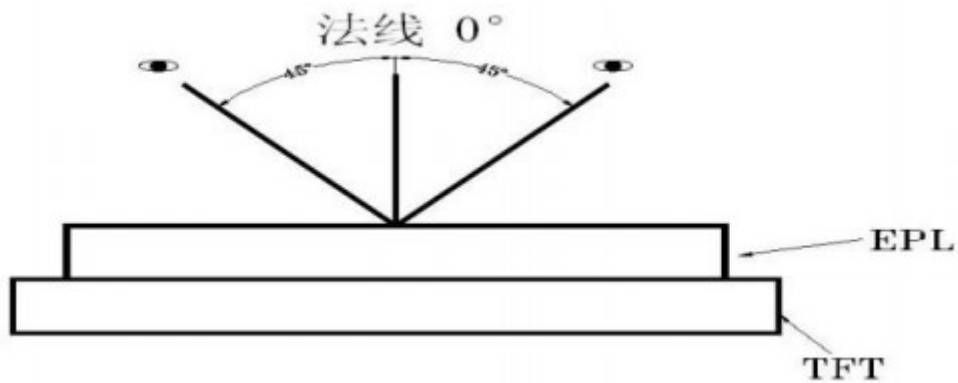
Temperature: 25 ± 3 °C

Humidity: $55 \pm 10\%$ RH

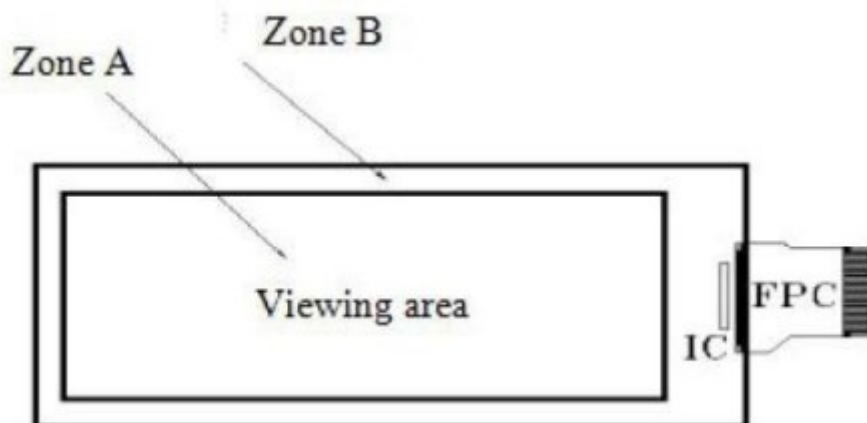
12.2 Illuminance

Brightness: 1200~1500LUX; distance: 30CM; Angle: Relate 45°surround.

12.3 Inspect method



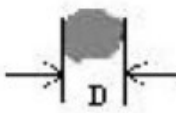
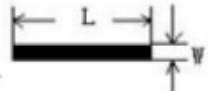
12.4 Display area



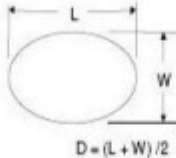
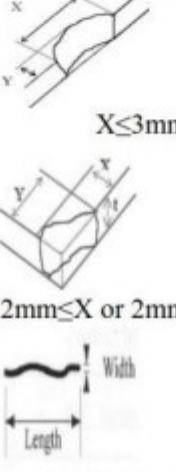


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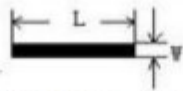
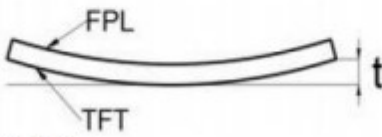
12.5 Inspection standard

13.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection	
2	Black/White spots	 $D \leq 0.3\text{mm}$, Allowed $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 3$, $0.5\text{mm} < D$ Not Allow	MI		
3	Black/White spots (No switch)	 $L \leq 1.0\text{mm}, W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}, W > 0.5\text{mm}$ is not allowed		Visual/ Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 <p>$D = (L + W) / 2$ $D \leq 0.3\text{mm}$, Allowed $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 5$ $D > 0.5\text{mm}$, Not Allow</p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 <p>$X \leq 3\text{mm}, Y \leq 0.5\text{mm}$ $2\text{mm} \leq X$ or $2\text{mm} \leq Y$ Allow $W \leq 0.1\text{mm}, L \leq 5\text{mm}, n \leq 2$ Edge crown: $X \leq 0.3\text{mm}, Y \leq 3\text{mm}$</p>	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	 Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 <p> $L \leq 1.0\text{mm}, W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}, W > 0.5\text{mm}$ is not allowed </p>	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	<p>TFT edge bulge: $X \leq 3\text{mm}, Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed</p>	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	<p> $D \leq 0.25\text{mm}$, allow $0.25\text{mm} < D \leq 0.4\text{mm}$, $n \leq 4$ allow $D > 0.4\text{mm}$ is not allowed ($n \leq 8$ items are allowed within 5 mm in diameter) </p>	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	<p>PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$</p>	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	<p>Edge Adhesives $H \leq$ PS surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble; bubble Width $\leq 1/2$ Margin width; Length $\leq 0.5\text{mm}$. $n \leq 5$</p>	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	Zone B
14	Silicon glue	<p>Thickness \leq PS surface (With protect film): Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised.</p>	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 <p> $t \leq 1.5\text{mm}$ </p>	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

13. Packaging

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